AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. (Currently Amended) A method of operating a computer system that includes first and second processors and memory shared thereby, the method comprising:

concurrently executing first and second instructions on respective ones of the first and second processors, the first and second instructions each attempting to reserve ~~reserving~~ in a same predefined order plural respective locations of the memory,

wherein, for at least the first instruction, selectively signaling of a fault corresponding to a later ~~reserved~~ one of the respective locations depends on a value read from an earlier reserved one of the respective locations.

2. (Original) The method of claim 1,

wherein the predefined order is in accordance with a fixed total order of locations within the memory.

3. (Original) The method of claim 1,

wherein the predefined order is one of ascending and descending memory address order.

4. (Original) The method of claim 1,

wherein the reserving includes locking an associated cache-line.

5. (Original) The method of claim 1,

wherein the reserving locks at least the respective location, but substantially less than all the memory.

6. (Original) The method of claim 1,

wherein the first and second instructions are linearizable synchronization operations.

7. (Original) The method of claim 1,

wherein the first instruction is a double compare-and-swap instruction.

8. (Original) The method of claim 1,

wherein the first instruction is a compound compare-and-swap instruction;

wherein the respective locations reserved by the compound compare-and-swap instruction number N; and

wherein signaling of a fault corresponding to a later reserved one of N locations depends on at least one value read from an earlier reserved one the N locations.

9. (Original) The method of claim 1,

wherein the first instruction is a double compare-and-swap instruction; and

wherein, unless a value read from the earlier reserved one of the respective locations compares to a corresponding test value, no fault corresponding to the later reserved one of the respective locations is signaled.

10. (Original) The method of claim 1,

wherein the execution of the first instruction includes access to the earlier reserved one of the respective locations; and

wherein, unless the access succeeds, no fault corresponding to the later reserved one of the respective locations is signaled.

11. (Original) The method of claim 1, wherein the execution of the first instruction includes

a first access corresponding to an earlier reserved one of the respective locations; and

an optional second access that signals a fault only if the first access succeeds.

12. (Original) The method of claim 1,

wherein the respective locations reserved by the first and second instructions are disjoint; and

wherein the concurrent execution is non-blocking.

13 – 46: (Cancelled)

47. (Currently Amended) A method of operating a computer system that includes a memory shared by plural processors thereof, the method comprising:

in response to execution of a single instruction by one of the processors,

separately attempting to reserve ~~reserving~~ plural locations of the memory prior to accessing contents of any one of the successfully reserved memory locations; and

selectively signaling a fault corresponding to a later ~~reserved~~ one of the locations based on a value read from an earlier reserved one of the locations.

48. (Original) The method of claim 47,

wherein, unless the value read from the earlier reserved location compares to a corresponding test value, no fault corresponding to the later reserved location is signaled.

49. (Original) The method of claim 47,

wherein the separately reserving includes separately locking at least the plural locations, but substantially less than all the memory.

50. (Original) The method of claim 47,

wherein the computer system further includes cache storage; and

wherein the separately reserving includes separately locking respective cache lines associated with the plural locations.

51. (Original) The method of claim 50,

wherein the cache storage includes a coherently maintained set of caches including ones respectively associated with each of the plural processors.

52. (Original) The method of claim 47,

wherein the instruction implements a compound Compare-and-swap (nCAS) operation.

53. (Original) The method of claim 47,

wherein the instruction implements a Double Compare-and-swap (DCAS) operation.

54. (Original) The method of claim 47,
wherein at least one of the plural locations is identified by an operand of the instruction.

55. (Currently Amended) A method of operating a processor, the method comprising:
in response to execution by the processor of a single instruction that separately accesses plural memory locations,
separately attempting to reserve ~~reserving~~ a first and a second one of the plural memory locations prior to accessing contents of either of the successfully reserved memory locations;
accessing the first one of the memory locations; and
selectively signaling a fault corresponding to the second one of the memory locations depending on a result of the first memory location access.

56. (Previously Presented) The method of claim 55, further comprising:
in response to the execution of the single instruction,
detecting the fault as part of the second memory location reservation; and
signaling the fault, if at all, only upon success of the first memory location access.

57. (Original) The method of claim 55,
wherein the first memory location access includes comparing a value read from the first memory location to a corresponding test value; and
wherein the signaling is performed, if at all, only upon success of the comparing.

58. (Previously Presented) The method of claim 55, further comprising:
signaling the fault corresponding to the second memory location, if at all, based on a value read from the reserved first memory location.

59. (Currently Amended) A processor that implements an instruction that separately attempts to reserve ~~reserves~~ a first and second memory locations prior to accessing contents of either of the first and second memory locations, and that addresses the first and second memory locations but for which signaling of a fault corresponding to the second memory location depends on a value read from the first reserved memory location.

60. (Original) The processor of claim 59,
wherein, unless the value read compares to a test value, no fault corresponding to the second memory location is signaled.

61. (Original) The processor of claim 59,
wherein the instruction is a compound compare-and-swap instruction.

62. (Previously Presented) The processor of claim 59,
wherein the fault, if any, corresponding to the second memory location is detected upon reservation thereof, but signaled, if at all, based on the value read from the reserved first memory location.

63. (Previously Presented) A computer program product encoded in at least one computer readable medium, the computer program product comprising:
a set of instructions executable on a processor,
the set of instructions including at least one instance of an instruction directing the processor to separately reserve first and second memory locations prior to accessing contents of either of the first and second memory locations, and to access first and second memory locations but for which signaling of a fault corresponding to the second memory location depends on a value read from the first memory location.

64. (Previously Presented) The computer program product of claim 63,
wherein the fault, if any, corresponding to the second memory location is detected upon reservation thereof, but signaled, if at all, based on the value read from the reserved first memory location.

65. (Original) The computer program product of claim 63,
wherein the instruction further directs the processor to reserve the first and second memory locations in a predefined order in accordance with a fixed total order of memory locations.

66. (Original) The computer program product of claim 63,
wherein, unless the value read compares to a test value, no fault corresponding to the second memory location is signaled.

67. (Original) The computer program product of claim 63,
wherein the instruction is a compound compare-and-swap instruction.

68. (Original) The computer program product of claim 63,
wherein the at least one computer readable medium is selected from the set of a disk, tape or other magnetic, optical, or electronic storage medium and a network, wireline, wireless or other communications medium.

69. (Currently Amended) An apparatus comprising:
a memory store;
means for separately attempting to reserve, ~~reserving~~ in response to a single instruction, first and second locations of the memory store prior to accessing, in response to the single instruction, contents of the first and second locations of the memory store if successfully reserved; and
means for signaling, if at all, a fault corresponding to the second location based on a value read from the reserved first location.